In the Specification:

*In the Section titled "*BRIEF DESCRIPTION OF THE DRAWINGS" *please delete the current section and insert the following:*

-- FIG. 1 is a simplified and schematic perspective view of a portion of an integrated circuit chip having bonding wires attached to bond pads and connected to portions of a leadframe, according to prior art.

FIG. 2 is a simplified and schematic perspective view of a portion of an integrated circuit chip having a surface structure integrating the power distribution functions of circuit and leadframe, according to the invention.

FIG. 3 is a version of the perspective view of FIG. 2 showing detail of the power distribution lines.

FIG. 4 shows the use of solder balls as connections to the power distribution lines.

FIG. 5 shows the integrated circuit chip and power distribution lines relative to the leadframe upon which the chip is mounted. --

On page 14, in the first full paragraph, please delete the paragraph and insert the following:

-- FIG. 2 summarizes the innovations of the present invention in order to remedy the above-listed shortcomings of the known technology. FIG. 2 is a simplified and schematic perspective view of a portion of an IC chip, generally designated 200, with design and fabrication features disclosed by the present invention. Semiconductor substrate 201 has a first ("active") surface 201a and a second ("passive") surface 201b. The second surface 201b is attached to the chip mount pad (221 in FIG. 3 and FIG. 5) of a prefabricated leadframe (typically copper, copper alloy, iron-nickel alloy, invar, or aluminum, about 100 to 300 μm thick). Of the plurality of leads (usually 14 up to over 600), FIG. 2 depicts only the tips 220a and 220b of a few leadframe segments, which are employed for power supply and located in the proximity of the IC chip. FIG. 5 shows a plan

view of the leadframe 500 with the IC chip 502 mounted on the chip mount pad 221. --

On page 16, in the second paragraph, please delete the paragraph and insert the following:

-- The outermost metal 271 of the deposited lines 251 and 252 is selected from a material which is bondable (and solderable, see below). Electrical conductors (506 in FIG. 5) connect this outermost metal with the lead tips (504 in FIG. 5) of the leadframe. In FIG. 2, wire bonding (the wire is preferably pure or alloyed gold, copper, or aluminum with a diameter of about 20 to 30 µm) is chosen as the preferred technique for electrical interconnection. Balls 208 and 209 are attached to lines 251 and 252, respectively, and stitches 210 and 211 are attached to lead tips 220a and 220b, respectively. It is important for the present invention that recent technical advances in wire bonding now allow the formation of tightly controlled wire loops and loop shapes. By way of example, loop 240 in FIG. 2 is shown much more elongated than loop 241. Wire lengths of 7.5 mm or even more are achievable with today's bonders. Such advances can, for instance, be found in the computerized bonder 8020 by Kulicke & Soffa, Willow Grove, PA, U.S.A., or in the ABACUS SA by Texas Instruments, Dallas, TX, U.S.A. Moving the capillary in a predetermined and computer-controlled manner through the air will create a wire looping of exactly defined shape. For instance, rounded, trapezoidal, linear and customized loop paths can be formed. --

On page 17, in the first paragraph, please delete the paragraph and insert the following:

-- The preferred structure of the deposited power distribution metallization for lines 251 and 252 consists of a seed metal layer (272 in FIG. 3) attached to the protective overcoat 230 and the bottoms of the vias 260, followed by a first relatively thin stress-absorbing metal layer (273 in FIG. 3), a second, relatively thick stress absorbing layer (274 in FIG. 3), and finally an outermost bondable

metal layer (271 in FIG. 3). Preferably, the seed metal layer is selected from a group consisting of tungsten, titanium, titanium nitride, molybdenum, chromium, and alloys thereof. The seed metal layer is electrically conductive, provides adhesion to both the metallization of the IC active components and the protective overcoat, permits the exposed portions of its upper surface to be electroplated, and prevents migration of the subsequent stress-absorbing metals to the components metallization layers. The thickness of seed metal layer is between about 100 and 500 nm. Alternatively, the seed metal layer may be composed of two metal layers; an example for the second metal is copper, since it provides a suitable surface for subsequent electroplating. --

On page 19, in the second paragraph, please delete the paragraph and insert the following:

-- As pointed out above, the outermost line layer may be selected so that it is solderable. A solder ball can then be attached to it by standard reflow techniques. However, it was described in the above-cited U.S. Patent Applications # 09/611,623 and 60/221,051 that it is often advisable to employ an additional solder mask (400 shown in FIG. 4) or polyimide layer with an opening (402) for each solder ball (404) in order to keep the flip-chip bump in a defined area and shape during bump formation and subsequent attachment to an external package or board. --

On page 20, in the first paragraph, please delete the paragraph and insert the following:

For operating the signal inputs/outputs of the IC, additional windows in the protective overcoat are needed to expose the underlying contact pad metallization (508 in FIG. 5). Wire bond (510 in FIG. 5) or solder balls can then be affixed to these contact windows. These windows and their respective wire bonds are not shown in FIG. 2.